

WHAT IS CLAIMED IS

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1. A state indicating information setting circuit comprising:

10 a first state holding part for inputting thereto a signal indicating either a predetermined first state or a predetermined second state, holding the state indicated by said signal input and outputting said state;

15 a second state holding part for inputting thereto the signal output from said first state holding part, holding the state indicated by said signal input and outputting said state;

20 a first state comparing part inputting thereto a predetermined state detection signal and the signal output from said second state holding part, and outputting a signal indicating said predetermined first state to said first state holding part when the respective states indicated by the respective signals input are different from one another, and outputting a signal indicating said
25 predetermined second state when these states are same as one another;

30 a second state comparing part comparing the states of the respective signals output from said first state holding part and said second state holding part, and outputting a signal indicating said predetermined second state as a state detection signal clearing signal when the respective states indicated by said input signals are different from one another; and

35 a third state comparing part comparing the states of the respective signals output from said first state holding part and said second state

holding part, outputting a state detection signal
indicating said predetermined first state when said
states of the respective signals input are different
from each other, and outputting the state non-
5 detection signal indicating said predetermined
second state when said states are same as one
another.

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2. A state indicating information setting
circuit comprising:

a first state holding part inputting
15 thereto a signal indicating either a predetermined
first state or a predetermined second state, holding
the state indicated by said signal input, and
outputting said state;

a second state holding part inputting
20 thereto the signal output from said first state
holding part, and holding and outputting the state
indicated by said signal input, and outputting said
state;

a third state holding part inputting
25 thereto the signal output from said second state
holding part, and holding and outputting the state
indicated by said signal input, and outputting said
state;

a first state comparing part inputting
30 thereto a predetermined state detection signal and
the signal output from said second state holding
part, outputting a signal indicating said
predetermined first state to said first state
holding part when the respective states indicated by
35 the respective signals input are different from one
another, and outputting a signal indicating said
predetermined second state when these states are

same as one another;

5 a second state comparing part comparing
the states of the respective signals output from
said first state holding part and said second state
holding part, and outputting a signal indicating
said predetermined second state as a state detection
signal clearing signal when the respective states
indicated by said input signals are different from
one another; and
10 a third state comparing part comparing the
states of the respective signals output from said
first state holding part and said third state
holding part, outputting a state detection signal
indicating said predetermined first state when said
15 states of the respective signals input are different
from each other, and outputting the state non-
detection signal indicating said predetermined
second state when said states given are same as one
another.
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3. A state indicating information setting
25 circuit comprising:

a first state holding part holding a state
of an input signal, and outputting a signal
indicating said state thus held;

30 a second state holding part holding the
state of the signal output from said first state
holding part, and outputting a signal indicating
said state thus held;

a state inverting part responsive to a
predetermined state detection signal for outputting
35 to said first state holding part a signal indicating
a state which is different from the state indicated
by the signal output from said second state holding

part;

5 a state detection signal outputting part
comparing the states of the respective signals
output from said first state holding part and said
second state holding part, outputting the state
detection signal when said states are different from
one another, and outputting a state non-detection
signal when said states are same as one another; and

10 a state detection signal clearing part
comparing the states of the respective signals
output from said first state holding part and said
second state holding part, and outputting a state
detection signal clearing signal when said states
are different from one another.

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20 4. A state indicating information setting
circuit comprising:

a first state holding part holding a state
of an input signal, and outputting a signal
indicating said state thus held;

25 a second state holding part holding the
state of the signal output from said first state
holding part, and outputting a signal indicating
said state thus held;

30 a third state holding part holding the
state of the signal output from said second state
holding part, and outputting a signal indicating
said state thus held;

35 a state inverting part responsive to a
predetermined state detection signal for outputting
to said first state holding part a signal indicating
a state which is different from the state indicated
by the signal output from said second state holding
part;

a state detection signal outputting part
comparing the states of the respective signals
output from said first state holding part and said
third state holding part, outputting the state
5 detection signal when said states are different from
one another, and outputting a state non-detection
signal when said states are same as one another; and
a state detection signal clearing part
comparing the states of the respective signals
10 output from said first state holding part and said
second state holding part, and outputting a state
detection signal clearing signal when said states
are different from one another.

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5. A state indicating information setting
circuit comprising:
20 a first flip-flop circuit taking an input
signal when a register read out signal has an L
level;
a second flip-flop circuit taking a signal
output from said first flip-flop circuit when the
25 register read out signal has an H level;
a third flip-flop circuit taking a signal
output from said second flip-flop circuit when the
register read out signal has the L level;
a first exclusive-OR circuit performing an
30 exclusive-OR operation between an output of said
second flip-flop circuit and a predetermined state
detection signal, and outputting a result of the
exclusive-OR operation;
a second exclusive-OR circuit performing
35 an exclusive-OR operation between an output of said
first flip-flop circuit and an output of said second
flip-flop circuit, and outputting a result of the

exclusive-OR operation; and

5 a third exclusive-OR circuit performing an exclusive-OR operation between an output of said first flip-flop circuit and an output of said third flip-flop circuit, and outputting a result of the exclusive-OR operation as a state bit signal.

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6. A status bit setting circuit comprising:

15 an inverting output part generating an output which is inverted each time when a predetermined status is detected;

state inversion transition parts having states inverted in sequence by the output of said inverting output part; and

20 a status bit setting part setting a predetermined status bit by detecting a process of propagation of the inversion transition in said state inversion transition parts.

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7. The status bit setting circuit as claimed in claim 6, further comprising a status detection canceling part detecting the process of the inversion transition in said state inversion transition parts, and generating a signal canceling a status detection state.

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8. The status bit setting circuit as

claimed in claim 6, wherein:

5 said status bit setting part detects a
completion of the propagation of the inversion
transition and cancels the setting of the
predetermined status bit.

10 9. The status bit setting circuit as
claimed in claim 8, wherein:

15 said state inversion transition parts have
the states alternately inverted in sequence in
response to a rising edge and a decaying edge of a
predetermined read out signal

20 10. The status bit setting circuit
claimed in claim 6, further comprising a bus driver
enabling reading out of the predetermined status bit
externally only during an interval in which a
predetermined read out signal is active.